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Electrical discharge coating of nanostructured TiC-Fe cermets on 304 stainless steel

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ABSTRACT

The electrical discharge coating (EDC) process, as used for the development of TiC-Fe cermet coatings on 304 stainless steel, has been investigated as a function of increasing current (2–19 A) and pulse-on time (2–64 μs). Coating morphologies, comprising of a mixture of TiC, γ-Fe, ά-Fe and amorphous carbon, were characterised using the combined techniques of scanning electron microscopy (SEM), energy dispersive spectroscopy (EDS), X-ray diffractometry (XRD) and cross-sectional transmission electron microscopy (TEM). The developed coatings exhibited variable hardness values, up to an order of magnitude higher than that of the substrate, depending on the content and dispersion of nanostructured TiC particles within the Fe matrix. Coating hardness was found to increase with increasing current, but decrease under conditions of high pulse-on times, reflecting differences in the amount of TiC incorporated into the coatings. Optimised coatings were achieved using conditions of low processing energy which minimised the development of pores and cracks.

1. Introduction

Titanium carbide (TiC) is a hard refractory ceramic material [1], widely used as a reinforcing phase in Cr-, Co-, Ni-, Mo- or Fe-based metallic alloys to produce ceramic-metal (cermet) composites for a variety of applications [2,3]. TiC coatings are commonly applied as a protective material to improve surface integrity and hence part service life [4], owing to their excellent physical and chemical properties such as a high hardness, high wear resistance, low coefficient of friction, and high chemical and thermal stability [5]. TiC adopts a type B1-NaCl (fcc) crystal structure and exhibits a wide range of compositions depending on the percentage of carbon dissolved in the Ti phase [6].

TiC coatings with good mechanical properties may be produced using thermal or plasma chemical vapour deposition (CVD) or physical vapour deposition (PVD) [7,8]. However, CVD coatings are deposited usually at high (>500 °C) temperatures [7] which may affect the mechanical properties of the substrate. PVD may be performed at lower temperatures of ~200 °C, but coatings deposited by thermal evaporation or ion plating, for example, tend to suffer from poor adhesion [9]. Also, CVD and PVD are relatively expensive techniques, requiring vacuum chambers and complex operational procedures [10]. Conversely, surface modification using the electrical discharge coating (EDC) method, being a modification of electrical discharge machining (EDM), has gained attention due to its simplicity of operation, with only a powder metallurgy (PM) electrode required to create a hard cermet coating [11]. Conveniently, this technique is easily integrated within widely available EDM hardware.

In conventional EDM, the removing of material is achieved through the conversion of electrical energy into thermal energy through a series of high frequency, 10^3–10^6 Hz, discrete electrical discharges between two electrodes, with small gap distance of 10–100 μm, immersed in a medium of dielectric fluid. Prior to discharge, an open voltage is applied between the two electrodes, after which an ignition delay time occurs for dielectric breakdown, constituting the statistical time-lag required for the generation of initial electrons and the time for dielectric ionisation. This delay time varies and depends upon the conditions in the gap (Fig. 1) [12]. Breakdown develops from the acceleration of electrons towards the anode, with the source of electrons being either from the cathode under the applied field or stray electrons present in the gap. The electrons impact with neutral atoms and particles present in the dielectric fluid, creating positive ions and additional electrons which accelerate towards cathode and anode, respectively. Each spark generates a localised plasma channel with high temperature, estimated to be in the range ~8000–12,000 °C, and induces a large localised pressure on the scale of ~200 atm [13]. Fig. 2 presents an adaption of the EDM process with reference to EDC, with workpiece and tool electrode held at positive and negative potentials, respectively. Sparking leads to

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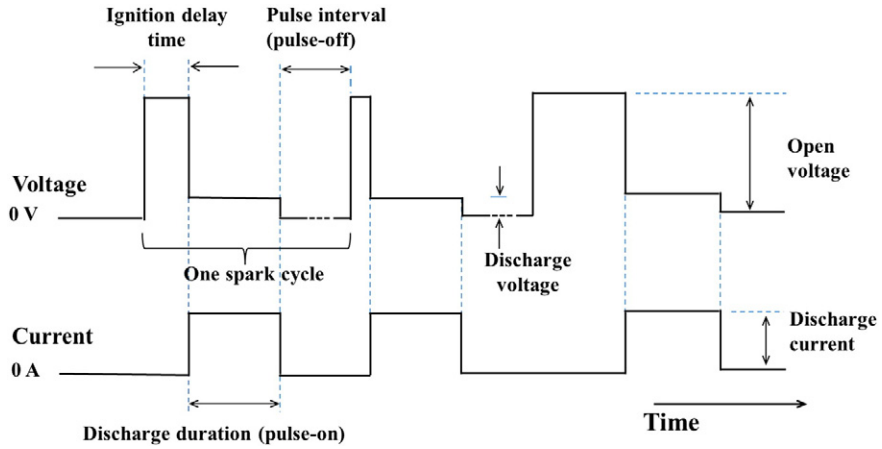

Fig. 1. Voltage and current waveforms during the electrical discharge process (adapted from [12]).

the development of localised melt pools on the surface of the workpiece which, when combined with TiC particles from the tool electrode, cool rapidly to form a localised cermet deposits. Multiple sparking events then allow multiple, overlapping craters to form a continuum coating across the workpiece.

ED processing may employ a PM tool electrode to form a TiC-Fe cermet coating on steel. For example, Suzuki and Kobayashi [14] have shown, from an investigation of single spark pulses, that the EDM process with reversed polarity can be used to develop a TiC coating onto high speed steel, using a semi-sintered TiC electrode. Similarly, Wang et al. [11] deposited TiC onto a carbon steel workpiece using a Ti green compact electrode, following reaction with C from the dielectric oil, as confirmed by X-ray diffractometry (XRD), reporting Vickers hardness over 2000 HV with 4.3 A and 8 μs on-time. In particular, these coatings exhibited hardness levels more than three times that of the substrate. Further, Hwang et al. [15] demonstrated that EDC using a multi-layered Ti/graphite electrode facilitated the development of TiC coatings on a Ni workpiece with reduced micro-crack formation, and a maximum hardness of 1710 HV.

In this context, there is for a requirement for EDC process optimisation and improved understanding of the mechanisms of cermet layer formation. Here, we report on the creation of a process-map for the EDC of TiC-Fe on 304 stainless steel, as a function of increasing current and pulse-on times. 304 stainless steel is used commonly across a range of engineering applications and provides an appropriate template for the appraisal of EDC processing phenomena.

2. Materials and methods

A 304 stainless steel workpiece (20 × 20 × 6 mm) was sequentially mechanically polished to a mirror finish concluding with 1 μm diamond paste and washed with acetone. A die sinking machine (Mitsubishi EA12V) was used to coat the workpiece using a PM TiC tool electrode (Ryoden Koki Engineering Co., Ltd.) (10 × 20 × 100 mm) and a dielectric fluid (Shell Paraol 250). ED coatings were investigated as a function of current (A) and pulse-on time (μs) which are known to affect the processed surface characteristics [16]. The process parameters of electrode polarity, voltage, pulse-off time and total machining time were fixed, as summarised in Table 1, in addition to an ignition delay time which is gap condition dependent, i.e. the time taken for the formation of a plasma after application of the gap voltage. This study reports on a set of 11 specimens, as a function of EDC processing, with one or two specimens for each set of processing conditions utilised for the characterisation experiments. All samples were EDC processed for 60 min. For the purpose of determining spark diameters, the sample set was replicated, for ~30 s of machining time, using identical processing parameters.

The tip of the TiC electrode was set to touch the top surface of the clamped workpiece, as a reference point, and retracted. The electrode was then advanced towards the workpiece under servo-control, allowing the gap-voltage to rise until it became sufficient to ionise the dielectric oil, with short duration discharges in the electrode gap leading to localised material coating and alloying of the workpiece.

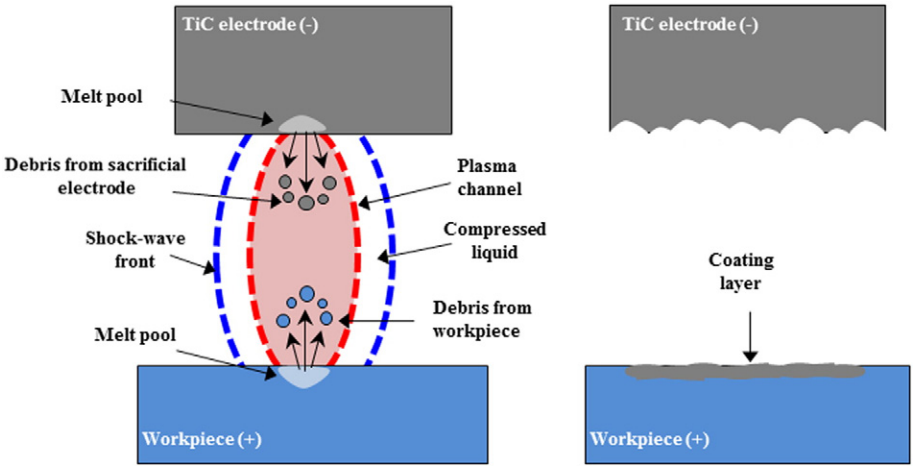

Fig. 2. Schematic representation of the EDC mechanism: a) plasma channel formation; and b) workpiece surface modification/coating, following many sparking events.

Table 1
EDC machining parameters.

Working parameters	Current/A (fixed pulse-on time of 8 μs)	Pulse-on/μs (fixed current of 10 A)	Pulse-off/μs	Open voltage/V	Tool electrode polarity	PM electrode	Machining time/minutes
Description	2,6,10,14,19	2,4,8,16,32,64	256	320	negative	TiC	0.5 and 60

Metallurgical analyses of the starting electrodes and processed workpiece surfaces were performed using scanning electron microscopy (SEM) (FEI XL30; 20 kV; spot size 4) and energy dispersive X-ray spectroscopy (EDS) (Oxford Instruments, INCA). Focused ion beam (FIB) milling (FEI Quanta 3D; 30 kV) was used to prepare sections of the coated samples for detailed investigation using cross-section using transmission electron microscopy (TEM) (JEOL 2100F, 200 kV). The structures of the processed samples were investigated using X-ray diffractometry (XRD) (Siemens D500; Cu Kα radiation (λ = 0.15406 nm); 40 kV and 25 mA; step size 0.02°; step time 2 s), with grain sizes estimated using the Scherrer equation. The chemical composition of the workpiece material was analysed also by spark emission spectrophotometry (Worldwide Analytical Systems AG, Foundry-Master; averaged over six different locations).

Bulk samples were cross-sectioned also using an ATA Brillant 220 cutting machine and then mounted, polished and washed with acetone and etched with Glyceregia solution (15 mL hydrochloric acid; 10 mL glycerol; 5 mL nitric acid) for observation using optical microscopy (Nikon Eclipse LV100ND with Nikon Digital Sight DS-Ri1 camera) to appraise the coating thicknesses (averaged from 40 locations). Box plot representation of this data includes a small box as mean, middle line as median, top and bottom of the large box as upper and lower quartiles respectively, whiskers as 99% of data, and small cross as absolute maximum and minimum values. Hardness measurements were performed using Vickers indentation with a load of 10 gf, using 8 measurements for each cross-section. Three dimensional optical profilometry (Talysurf series CLI 1000, Taylor Hobson), was used to investigate surface profiles and return average values for roughness R_a (n = 7), a surface area of 2 × 2 mm for each sample was evaluated, at a scan speed of 500 nm/s.

3. Results

3.1. Materials

A secondary electron (SE) image of the starting TiC tool electrode produced by PM sintering is presented in Fig. 3 showing the coarse particle structure, up to ~5 μm in size. An SE image of the initial polished 304 stainless steel workpiece is shown in Fig. 5a, revealing a very flat, uniform topography (R_a < 1 μm), whilst spark emission spectrophotometry returned the composition summarised in Table 2.

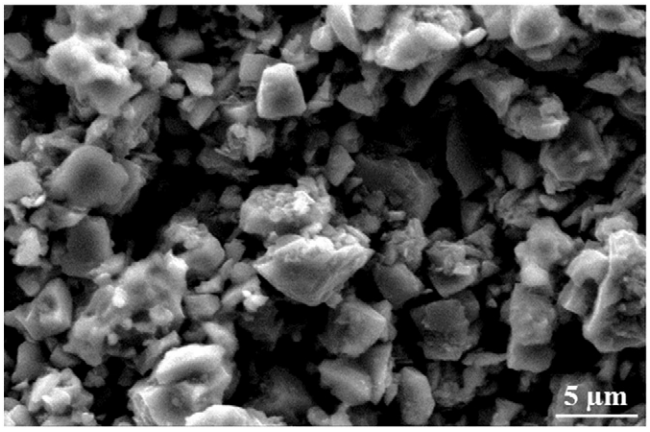

Fig. 3. SE image of starting TiC tool electrode.

XRD data for the tool electrode is presented in Fig. 4a, confirming TiC (EVA software card No. 00-032-1383), whilst Fig. 4b shows XRD data for the as-received and polished 304 stainless steel, confirming the dominance of γ austenite (fcc) and the presence of some α` martensite (bcc).

3.2. EDC processed materials

3.2.1. Effects of current and pulse-on time on surface topography

The surface quality and homogeneity of the coatings are dependent strongly on the discharge conditions. For example, Figs. 5 and 6 present low magnification SE images of the substrate and as-deposited coatings, as a function of increasing current (for fixed pulse-on time of 8 μs) and increasing pulse-on time (for fixed current of 10 A), respectively, showing significant changes in surface morphology.

Fig. 5b shows evidence for the development of individual TiC containing craters at the surface, when EDC processed with a current of 2 A. This sample showed low levels of micro-cracking and micro-porosity, with surface roughness of R_a = 3.8 μm. Occasional TiC-rich surface particles, confirmed by EDS, were observed also on the surface of this sample, being attributed to larger particles transported from the tool electrode.

Fig. 5c and d illustrate surfaces EDC processed with higher discharge currents of 6 and 10 A respectively, showing the onset and development of micro-cracks bounding the initially formed craters. These samples showed slightly increased surface roughness values of 3.9 μm, respectively. With further increases of current to 14 and 19 A, void and micro-crack formation became even more pronounced, although the locations of the craters could still be discerned. These samples both returned roughness values of 4.0 μm. In particular, it is noted that there was an increase in crater size with increasing processing current (Table 3).

Fig. 6 shows similarly the development of craters and surrounding micro-cracks for samples processed with increasing pulse-on time (fixed current of 10 A). For a short pulse duration of 2 μs, the processed surfaces showed low levels of void and crack formation (Fig. 6a), and returned a surface roughness value of 3.3 μm. Fig. 6b and c demonstrate the on-set and development of micro-crack formation bounding the craters with increasing pulse-on time, of 4 and 8 μs, respectively. Increasing the pulse-on time further to 16, 32 and 64 μs, respectively, led to increased void formation, with cracks widening and becoming elongated, and voids becoming larger and denser, being instrumental in extended, interconnecting crack formation (Fig. 6d–f). It was found that surface roughness increased slightly, reaching R_a = 5.0 μm, at 16 μs pulse-on time, but then decreased when the pulse-on time exceeded 16 μs.

Fig. 7 shows two characteristic features of these EDC processed surfaces, i.e. a pore at the substrate, formed under conditions of 19 A current (fixed 8 μs pulse-on time); and a surface particle, formed under conditions of 32 μs pulse-on time (fixed 10 A current). As the processing current became larger, it was observed that pores and cracks opened-up (Fig. 7a (1)), allowing the substrate to be detected by EDS, whilst the

Table 2
Chemical composition of the 304 stainless steel workpiece (n = 6).

	C	Si	Mn	Cr	Mo	Ni	Al	Co	Cu	V	W	Fe
Wt%	0.03	0.60	2.0	18.6	0.23	8.4	0.01	0.14	0.21	0.11	0.1	bal.

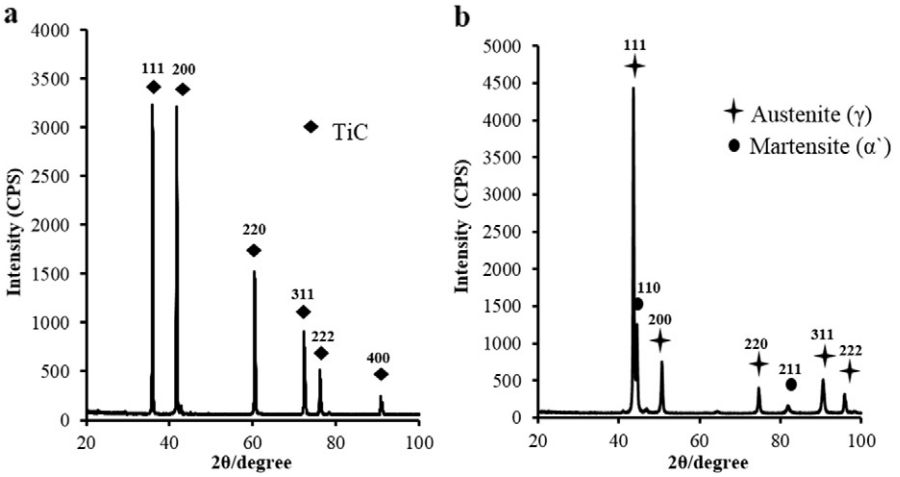

Fig. 4. X-ray diffraction data for the starting: a) TiC tool electrode; and b) 304 stainless steel substrate.

coating was found to be TiC-rich (Fig. 7a (2)). Conversely, large surface particles (Fig. 7b) were found to be carbon enriched TiC clusters, considered to originate from the PM electrode and reacting with carbon cracked from the dielectric fluid.

3.2.2. Layer thickness

The investigation of mechanically polished and chemically etched coatings, in cross-sectional geometry, showed large variations in layer thickness, as a function of process conditions. For example, the SE image of Fig. 8 shows the edge of a coated region of a sample processed under conditions of 6 A current and 8 μs pulse-on time. The developed coating has replaced and fused with the substrate in an irregular fashion.

Fig. 9a,b show optical microscope images and associated box plots for layer thickness, for the developed coatings, as a function of increasing current and pulse-on time, respectively. It is evident that the layers become thicker gradually (from ~7 to 10 μm) and more discontinuous as the current increases (from 2 to 19 A), whilst there is a much stronger increase in layer thickness (from ~3.6 to 34 μm) with increasing pulse-on time (from 2 to 64 μs).

3.2.3. Crystal structure

XRD analyses were performed to appraise the structural integrity of the coatings, as a function of process conditions. Fig. 10 presents XRD patterns as a function of increasing current (for fixed pulse-on time of 8 μs), confirming increasing incorporation of TiC in all the coatings with some slight preferred orientation. In addition, signatures for γ-Fe and ά-Fe phases were evident. A small peak attributable to amorphous carbon was found to develop with increasing current. Signatures due to low levels of Cr_3C_2 (01-071-2287) and Fe_3C (00-035-0772) were detected also.

Fig. 11 presents XRD patterns for these coatings as a function of increasing pulse-on time (for fixed current of 10 A), again showing the increasing dominance of TiC with some slight preferred orientation. The crystalline peaks became more intense and sharp with increasing discharge duration from 2 to 16 μs, consistent with the development of higher levels of coating crystallinity. However, beyond 16 μs pulse-on time, the peak intensity due to TiC reduced, whilst the signature due to amorphous graphite increased, indicating the development of coatings with lower levels of crystallinity. Very small signals attributable to the presence of Cr_3C_2 and Fe_3C again were detected.

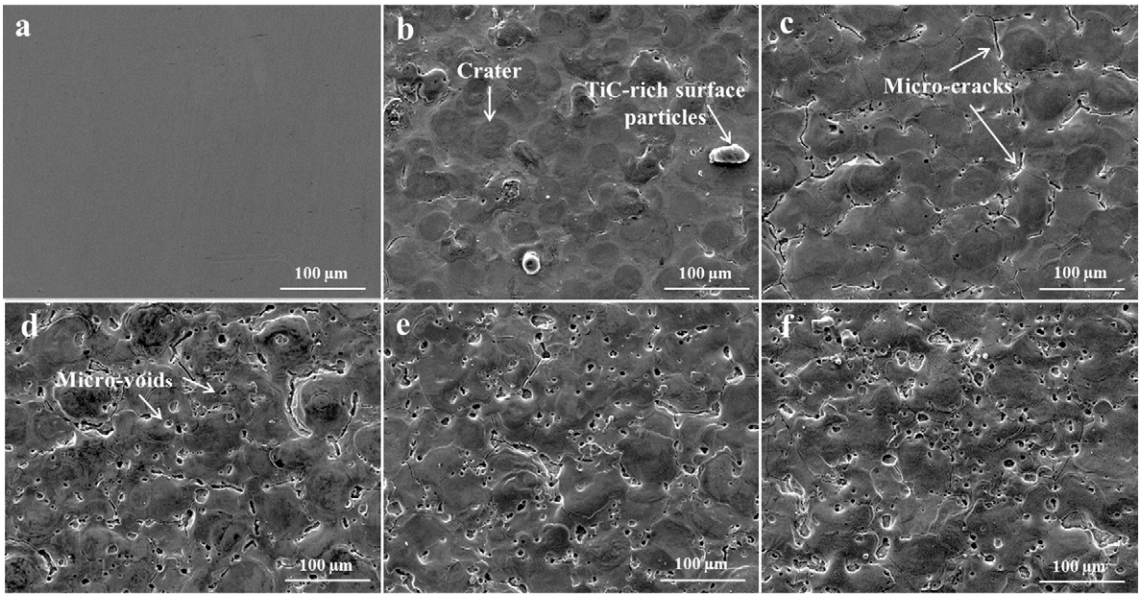

Fig. 5. SE images of: (a) polished 304 stainless steel; and (b-f) TiC-rich coatings deposited as a function of increasing current: 2, 6, 10, 14 and 19 A, respectively, for 1 h processing time and 8 μs pulse-on time.

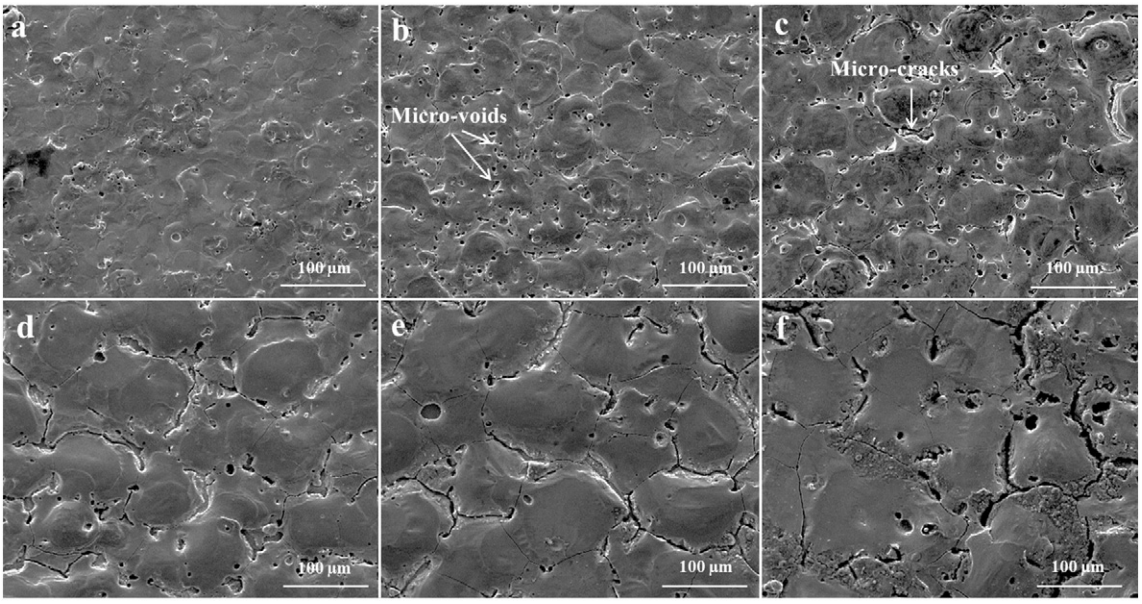

Fig. 6. SE images of: (a-f) Coatings deposited as a function of increasing pulse-on time: of 2, 4, 8, 16, 32 and 64 μs, respectively, for 1 h processing time and a fixed current of 10 A.

Fig. 12a,b present plots of averaged grain sizes, as determined from XRD data using the Scherrer equation, along with calculated energy values associated with each set of processing conditions, as a function of increasing current and pulse-on time, respectively. The grain size values reported relate to calculations made using the 111 diffraction peaks for TiC, whilst the associated error bars relate to the spread of grain sizes, as determined using 200, 220, 311and 222 diffraction peaks, indicating a wide spread of grain sizes and aspect ratios within the samples. In all cases the mean grain size values returned of ~ 40 nm were very much smaller than that of the ~130 nm grain size of the TiC in the tool electrode, again as determined using the Scherrer equation. Process energies were determined simply from the products of applied voltage, current and pulse-on times. It is noted that increasing process energies up to ~0.05 J led to an increase in average grain size, whilst further increases in energy led to a decrease in grain size.

3.2.4. Hardness

Fig. 13a, b present bar graphs of Vickers micro-hardness for the coatings in cross-section geometry, and associated plots of Ti wt% values from EDS investigations of these samples in planar-view (with compositional data acquired from representative areas of ~0.24 mm^2 for each sample). It should be noted that indents of samples produced using 2 A current and 2 μs on-time, were too thin to provide reliable hardness data, and hence were omitted from the data set shown. It is evident that there is a direct correlation between hardness and Ti (and TiC by implication) content within the cermet. Increasing the discharge current led to a progressive increase in TiC deposition (Fig. 13a), with consequent increase in tool electrode wear. These EDC processed layers exhibited hardness values ~4–8 times higher (from 6 to 19 A) than that of the stainless steel substrate (196 HV; σ = 16.8), demonstrating the ability of EDC processing to impart improved mechanical performance to the surface of austenitic stainless steel. However, an initial increase in hardness and Ti (TiC) content for increasing pulse-on time, up to 8 μs, was followed by a steady reduction in both hardness and TiC content for further pulse-on time increases. Coatings produced with 19 A current and 8 μs pulse-on time returned the highest mean value of hardness of ~1888 HV. It should be noted that some anomalous data points were observed during hardness testing, resulting in both high and low hardness results, attributable perhaps to extremely localised TiC deposits, i.e. inconsistent coating, and porosity, respectively.

3.2.5. Cross-sectional TEM

In order to gain insight into the fine-scale microstructure, Fig. 14 presents a TEM cross-section, prepared by FIB milling, showing the variability of cermet structure into the depth of the coating. The FIB specimen was prepared using Ga + ions at 30 kV, with sequential reduction in beam current density until it became electron transparent. A final stage of sectioning produced a window, ~2 μm wide, of very thin material for high resolution imaging and detailed chemical analysis. This "lift-out" sample was transferred to the TEM support grid using a nanomanipulator (OmniProbe 100). It is evident that there are several broad bands of coating material, with small, ~20–80 nm, equiaxed TiC grains at the near surface (Fig. 14(a)-I), as measured using ImageJ; a transition zone of larger, ~30–110 nm sized TiC grains (II); a region of columnar grains of length ~330–450 nm and width ~90–140 nm (III); and intermediate sized TiC grains ~150–800 nm (IV) towards the coating/substrate interface. Fig. 14(d) shows a phase contrast image of the

Table 3
Summary of individual crater sizes (n = 30), continuum layer surface roughness values (n = 7), cermet layer thicknesses, and coating Ti wt% values, as a function of increasing current and pulse-on time.

	Current/A					Pulse-on time/μs					
	2	**6**	**10**	**14**	**19**	**2**	**4**	**8**	**16**	**32**	**64**
Mean crater size/μm	**41**	**60**	**69**	**83**	**96**	**35**	**57**	**69**	**107**	**151**	**165**
σ	*4.3*	*4.7*	*5.0*	*8.6*	*8.7*	*5.6*	*11.8*	*5.7*	*7.8*	*14.3*	*16.5*
Mean surface roughness Ra/μm	**3.8**	**3.9**	**3.9**	**4.0**	**4.0**	**3.3**	**3.9**	**3.9**	**5.0**	**4.5**	**4.3**
σ	*0.5*	*0.6*	*0.7*	*0.6*	*0.4*	*0.6*	*0.6*	*0.7*	*0.4*	*0.5*	*0.6*
Mean cermet layer thickness/μm	**7.0**	**8.0**	**10.4**	**11.6**	**10.0**	**3.6**	**7.9**	**10.4**	**11.9**	**16.0**	**34.0**
Coating Ti content/wt%	**30.6**	**28.5**	**40.3**	**42.8**	**46.5**	**26.7**	**42.9**	**40.3**	**36.3**	**22.9**	**20.4**

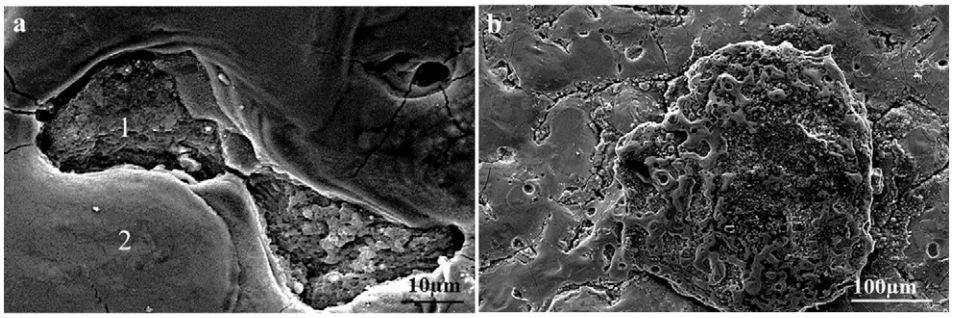

Fig. 7. High magnification SE images showing details of: (a) a pore formed under conditions of 19 A current (fixed 8 μs pulse-on time); and b) a large surface particle formed under 32 μs pulse-on time (fixed 10 A current).

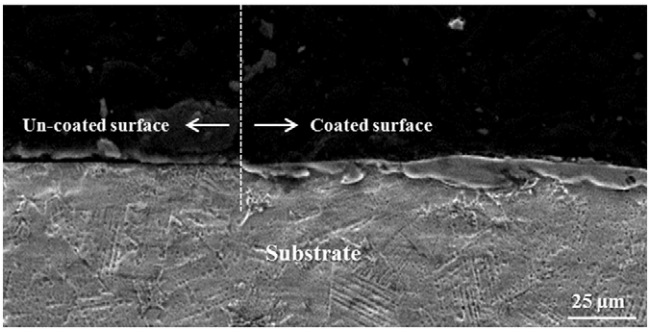

Fig. 8. SE image of a coating, viewed in cross-section, EDC processed with 6 A current and 8 μs pulse-on time.

grains at the surface with lattice spacing again consistent with the development of TiC ($d_{111} = 0.246$ nm; $d_{220} = 0.154$ nm).

Figs. 15 and 16 provide more details of the near surface structure and chemistry. Fig. 15 presents an annular dark field scanning TEM (ADF-STEM) image of the near surface grains with associated convergent beam electron diffraction (CBED) patterns consistent with the presence of fcc TiC grains ((1) systematic row and (2) close to ⟨110⟩ projection), within a matrix of iron ((3) systematic row), along with some localised clusters of amorphous C (4).

Fig. 16 presents an ADF-STEM image of the same region with associated EDS chemical maps showing the distribution of elemental Ti, Fe, C and Cr, respectively, within this cermet. The data shows the phase separation of TiC grains within a Fe-rich matrix along with a cluster of C-rich deposits. Interestingly, there is also strong evidence for a fairly uniform distribution of Cr throughout the sample, slightly enhanced within the Fe matrix.

4. Discussion

The significant variation in the hardness of TiC-Fe nanostructured coatings, as a function of current and pulse-on time, emphasises the importance of EDC process control. Considerable variation in coating topography, composition and fine-scale structure has been revealed depending on the amount of energy supplied to the surface. Each

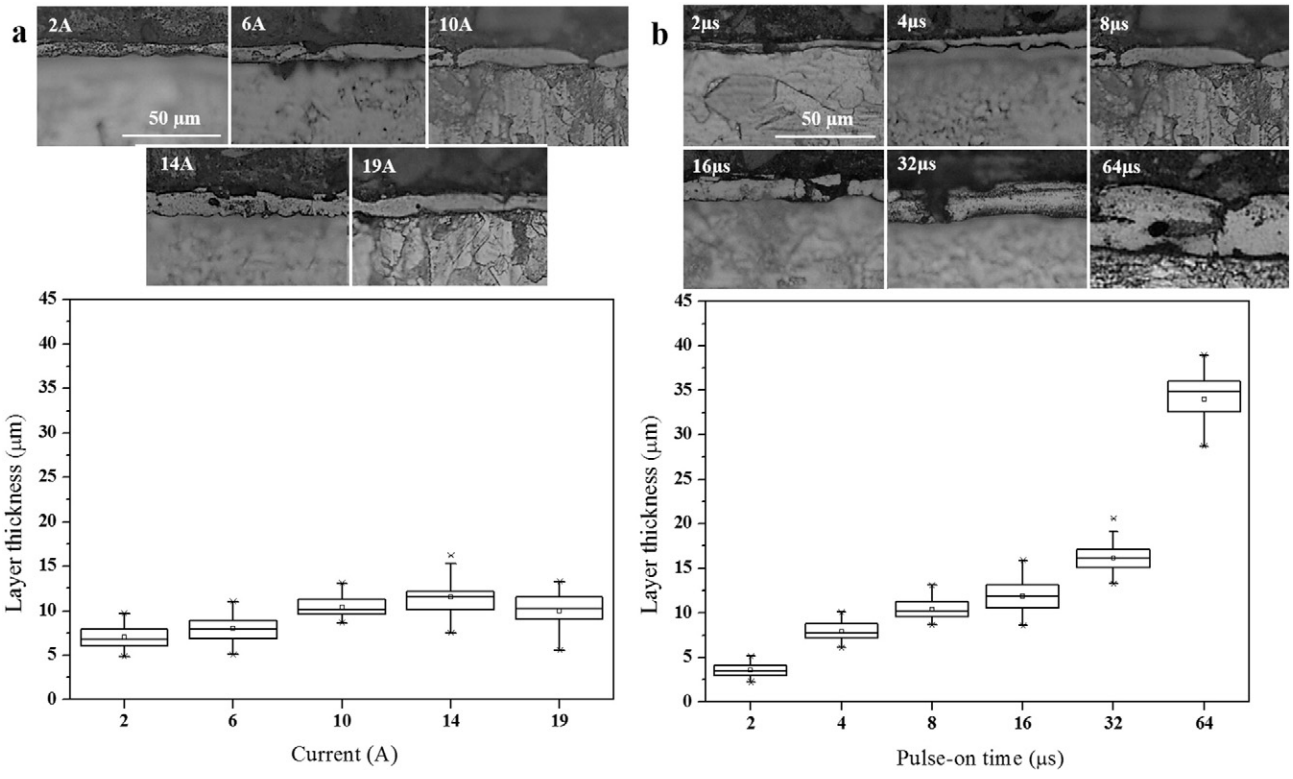

Fig. 9. Variation of coating layer thickness (μm) as a function of: a) increasing current (A); and b) increasing pulse-on time (μs) (n = 40).

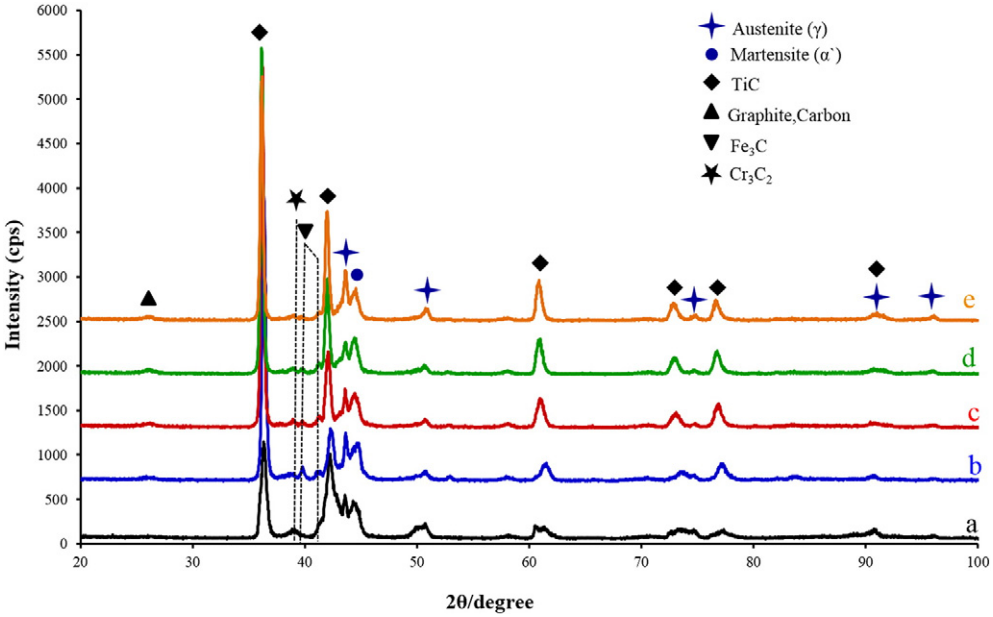

Fig. 10. XRD patterns of coatings produced under conditions of 8 μs pulse-on time and increasing current: a) 2 A, b) 6 A, c) 10 A, d) 14 A, and e) 19 A, respectively.

spark creates a localised melt pool which allows the fusion of TiC from the tool electrode with substrate material, which then rapidly cools and solidifies during the next pulse-off time.

The crater sizes, which range from ~35 to 165 μm (Table 3), are dependent on input energy which increases with increasing current and pulse-on time, consistent with other related work [17]. All samples were processed for 1 h, during which time an effective area of ~200 mm^2, equating to the combined area of ~9.4×10^3 to 208×10^3 craters, was exposed to a total of ~8.6×10^6 to 10.1×10^6 sparks, returning spark numbers of ~48 to 916 for each location (Table 4). These calculations cover the range of processing currents, on-times and off-time used here, in addition to an estimated value for the ignition delay time, determined as ~100 μs [18]. The point being that every part of the workpiece surface has experienced the effects of the repeated creation of many localised melt pools and solidification events, from this multiple sparking process, to create a continuum cermet TiC-Fe coating. It should be noted that the SE images reveal the distribution of individual craters corresponding to the final sequence of sparks as the plasma bombards the workpiece surface [19]. It is considered that the clustered distribution of craters reflects pathways of least resistance to sparking arising from localised difference in electrical conductivity of the substrate and statistically this variability promotes uniform coverage of the workpiece surface.

Surfaces produced with the lowest current (2 A) or lowest pulse-on time (2 μs), i.e. low input energy, exhibited the lowest number of voids and cracks (Figs. 5&6). In particular, the size of the craters was found to

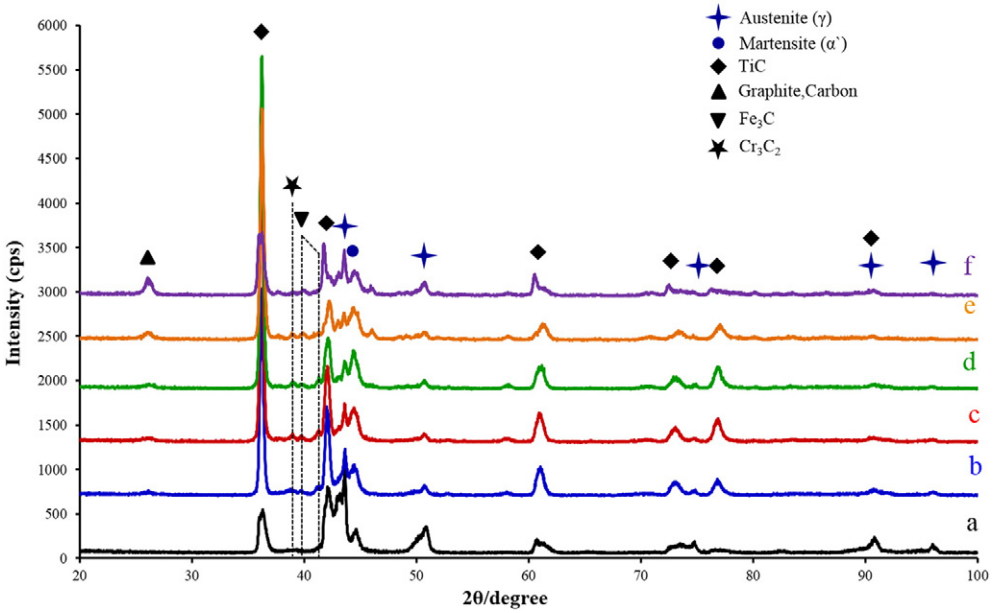

Fig. 11. XRD patterns of coatings produced under conditions of 10 A and increasing pulse-on times: a) 2 μs, b) 4 μs, c) 8 μs, d) 16 μs, e) 32 μs, and f) 64 μs, respectively.

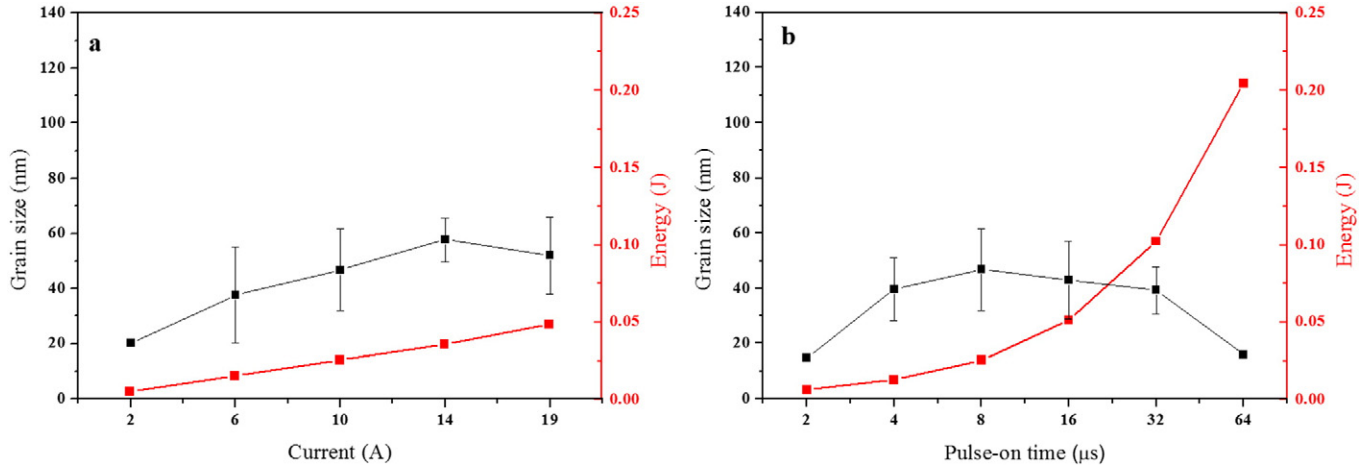

Fig. 12. TiC grain size values and calculated input energy as a function of: a) current (A); and b) pulse-on time (μs).

increase with increasing current and pulse-on time (Table 3), along with an increased tendency for void and crack formation [20], and a consequent increase, generally, in surface roughness. Again, this reflects the impact of increasing energy into the surface, combined with variations in the amount of Ti content retained within the coatings (Table 3 & Fig. 13), and the consequences of rapid cool down, with differential thermal contraction leading to coating disruption and crack formation [21], localised around crater edges. In addition, it is noted that there is a significant difference in the melting point of the coating and the substrate material, with the melting point of TiC (3430 K) being slightly higher than the boiling point of iron (3023 K), and hence Fe remains molten whilst TiC becomes recast during the initial stages of cermet solidification [22]. The associated effect of porosity formation may be attributed to the expulsion of gas bubbles to the surface from molten material during solidification [23].

It is evident that there is an association between increasing energy input into the surface and an increase in average grain size. However, the significant variations in coating hardness (Fig. 13a,b), as a function of increasing current and pulse-on time may be attributed to variations in the Ti wt% (and hence TiC) content [15,24], within the developed coatings (Fig. 13), rather than due to trends in the grain size. The lowest values of hardness were returned for conditions of low current, but current conditions of 6 A produced a coating ~4 times harder than the substrate [15]. Maximum values for hardness were achieved using the highest processing current of 19 A, being ~8 times harder than the substrate. However, these layers showed the highest levels of cracking and void formation which are undesirable. Progression into the regime of higher pulse-on times, and even higher processing energy conditions, led to a reduction in coating hardness, attributable primarily to a reduction in the Ti content, combined with increased carbon incorporation. The suggestion, therefore, is that high energy conditions equate to a case of 'over-processing' and that reduced conditions of current and pulse-on time are desirable for optimised material functional properties, in this case hardness, free of the deleterious effects of cracking and void formation. In this context, it is recognised that the amount of transformed TiC can be defined by controlling the process parameters of discharge current and pulse-on time [22]. For the TiC-Fe system reported here, the data suggests optimised EDC process conditions around 2–10 A and ~2–8 μs.

The characterisation data revealed a range of further interesting insights into the development of these cermet coatings. XRD analysis demonstrated the presence of predominantly γ austenite and some α`martensite within the substrate, and comparable levels of martensite compared to austenite within the cermet coatings, being indicative of the rapid cooing rates associated with the EDC process. Further, the XRD data demonstrates the TiC grains within the coating are significantly smaller than those within the tool electrode, which demonstrates that the TiC material transported to the coating layer achieved a fully molten state prior to solidification. This description of the complexity of the cermet coating is reinforced by the TEM investigation of the sample processed under the intermediate conditions of 10 A and 8 μs, demonstrating further the complex size distributions and aspect ratios of

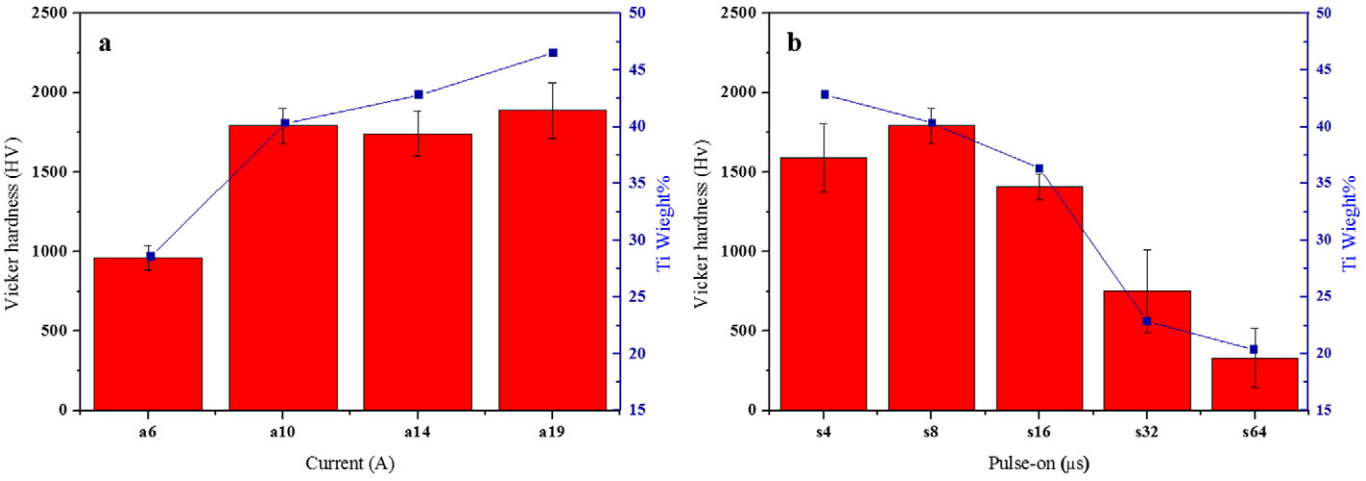

Fig. 13. Vickers hardness and Ti wt% values, as a function of: a) current (A); and b) pulse-on time (μs), error bars are the standard deviation of the 8 measurements.

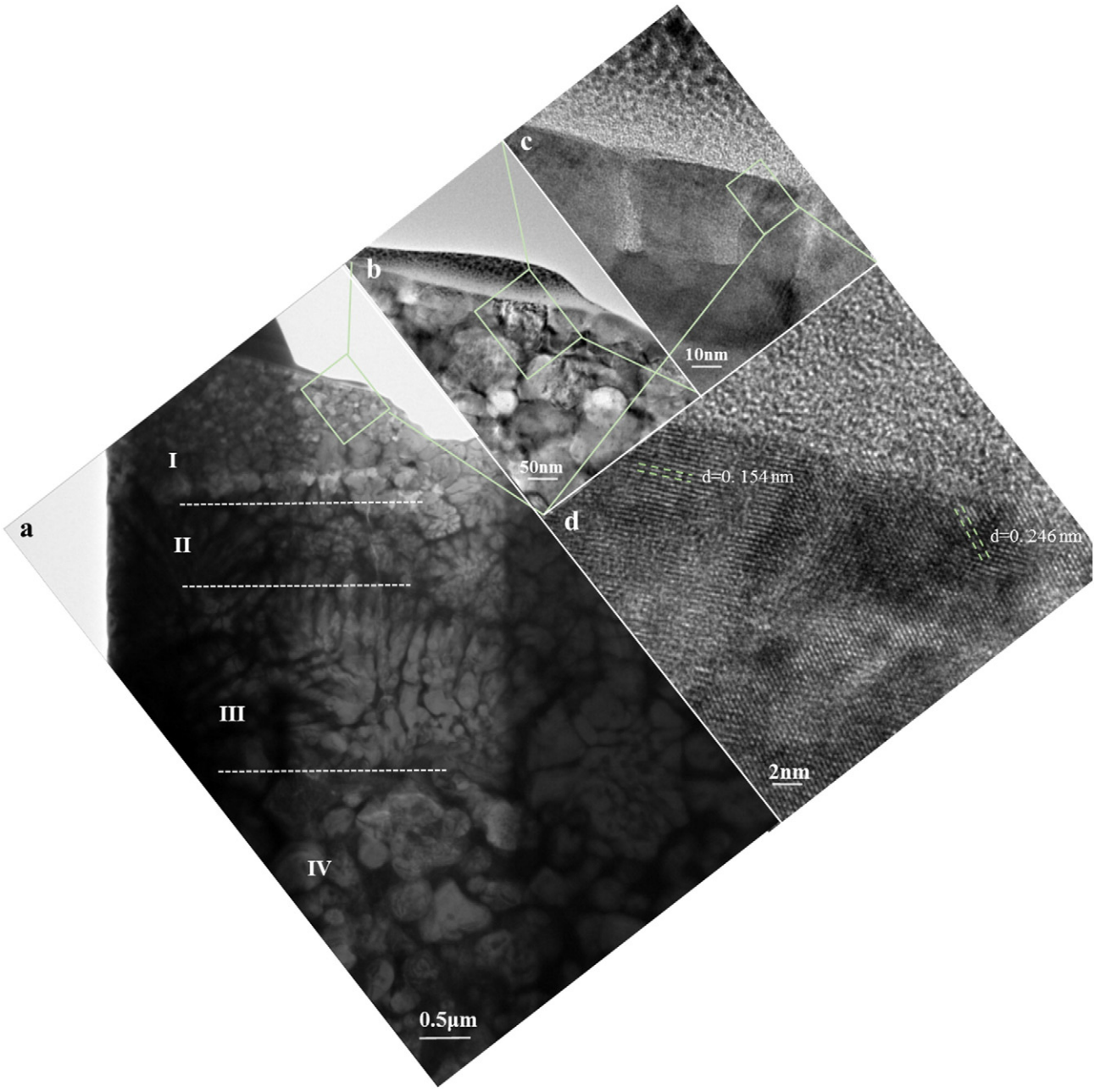

Fig. 14. Cross-sectional TEM micrograph of an EDC layer processed under conditions of 10 A and 8 μs: (a) large field of view; (b-d) near surface region at increasing levels of magnification (boxed regions in each respective images).

these nanostructured TiC grains within these coatings [25], reflecting the directions of solidification and grain growth during rapid cooling [26]. A narrowing of TiC peaks within the XRD data for increasing current and pulse-on conditions indicates an increase in averaged grain size with increasing energy into the surface. Further, both XRD and EDS data indicated a reduction in the TiC content within the developed coatings with increasing pulse-on time and an associated increase in carbon content from the cracked dielectric oil under higher energy processing conditions. The lack of correlation of grain size with the trend in hardness confirms that the coating hardness is determined by TiC wt% content.

With reference to the binary Ti-C phase diagram, carbon concentrations between 10 and 19.3 wt% C constitute primary TiC during solidification, i.e. TiC is stable over a wide range of compositions. When the carbon content exceeds 19.3 wt%, graphite begins to form and this effect is seen here for the case of high energy processing conditions with the formation of graphite (Figs. 10 & 11) and small regions of amorphous carbon (Figs. 15 & 16), based on XRD and TEM data, respectively. The small peaks in the XRD data attributable to the presence of minor levels of Cr_3C_2 and Fe_3C are at levels which are unlikely to affect the functional properties of these cermet coatings.

The TiC-rich particles (Fig. 5b) identified on the processed surfaces under conditions of low current were attributed to partially melted TiC deposited directly from the tool electrode, also resulting in non-uniformity of TiC in the coating. Conversely, the surface particles (Fig. 7b) formed under high pulse-on conditions were found to be very C-rich and hence attributed to TiC particles alloyed with cracked C from the dielectric fluid.

It is noted that there is a trend for increasing cermet coating layer thickness with increasing input energy into the surface. Consistent with the observation of increased recast layer thickness in EDM processed materials with increasing current and pulse-on conditions [27].

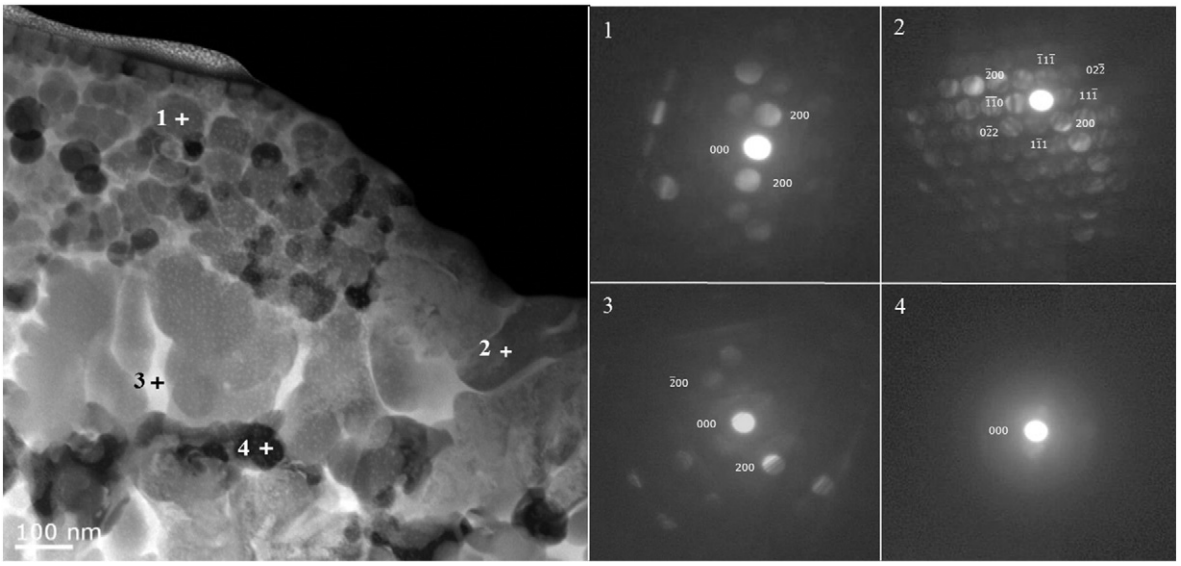

Fig. 15. ADF-STEM image of the near surface grain structure; with associated CBED patterns from the specified locations consistent with (1, 2) TiC; (3) Fe and (4) amorphous C.

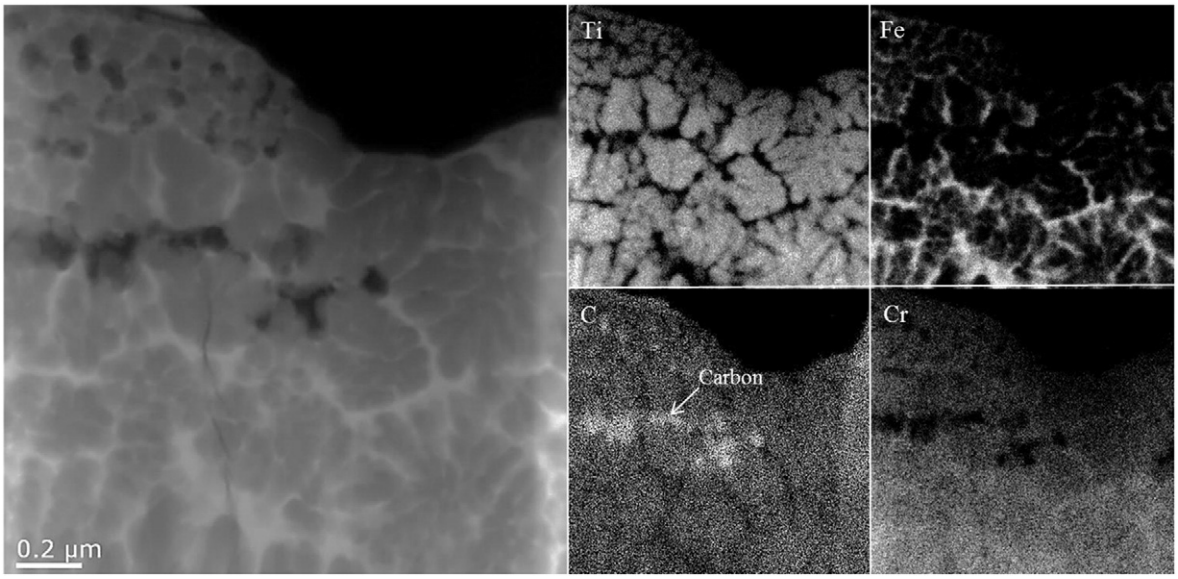

Fig. 16. ADF-STEM image with associated elemental maps showing the dispersion of Ti, Fe, C and Cr.

Further, it has been reported that increased pulse-on time results in both increased residual stress and recast layer thickness which can promote crack formation [28], consistent with observations made here.

In summary, it is likely that the processing conditions for the EDC technique will need to be optimised for any particular materials system and perhaps geometry. Nevertheless, there are a number of important trends emerging from this study, all of which point towards the benefits of low energy processing conditions, for effective application across a wide range of potential applications in wear and corrosion resistant coatings.

5. Conclusions

This investigation of EDC processed TiC-Fe cermet coatings on 304 stainless steel substrates has focused on the key process parameters of

Table 4
Estimate of the total number of sparks experienced by each location during the EDC process, emphasising that every location undergoes repeated melt pool formation and solidification, after 1 h, to create each continuum TiC-Fe cermet coating.

	Current/A					Pulse-on time/μs					
	2	6	10	14	19	2	4	8	16	32	64
Total number of sparks to cover surface ($\times 10^3$)	152	71	54	37	28	208	78	54	22	23	9.4
Total number of sparks during process ($\times 10^6$)	9.9	9.9	9.9	9.9	9.9	10.1	10.0	9.9	9.7	9.3	8.6
Total number of sparks per location	65	140	185	267	358	48	128	185	435	409	916

current and pulse-on time. The data reflects the sequence of repeated localised melt pool formation and solidification of intermixed TiC originating from the tool electrode with substrate material, until continuum cermet layer coverage is established. The data demonstrates variable hardness of these nanostructured coatings which relates primarily to variation in the TiC content within the developed coatings which contain complex intermixtures of TiC, γ-Fe, ά-Fe and graphite/amorphous carbon, along with trace levels of Cr_3C_2 and Fe_3C, reflecting the input energy and high cooling rates. It is evident that layers can become over-processed under conditions of high input energy, characterised by increased levels of void formation and cracking around crater edges, along with reduced levels of TiC incorporation and increased levels of carbon from cracking of the dielectric oil. Hence, the suggestion is for the use of reduced energy conditions for process optimisation, around 2–10 A and ~2–8 μs, for this materials system, promoting good levels of hardness and better surface finish with reduced levels of voids and cracks.

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